REMARKS

This communication responds to the Final Office Action mailed on January 7, 2004. At the time of the Office Action, claims 1-42 were pending. In the Office Action, claims 1-9 were allowed, and claims 10-33 and 35-42 were rejected. Claim 34 was indicated as being allowable, but was objected to as being based on a rejected claim.

Herein, claims 10 and 29 are amended.

Please reconsider the claims in view of the following comments.

INTERVIEW SUMMARY

The arguments of Sections A and B below, and the amendments to claims 10 and 29 made above, were sent in draft form to the Examiner by facsimile on March 9, 2004. In the Interview held on March 15, 2004, the Examiner stated that he found the arguments persuasive, especially concerning the undersigned's view that Lin's process would be destroyed by the proposed modification. Notwithstanding the persuasiveness of the arguments, he also suggested that the amendments proposed to claims 10 and 29 be made.

Again, thanks to the Examiner for his courtesy in allowing the Interview and for allowing the amendments to claims 10 and 29.

A. The Rejection of Claims 10-33 and 35-42 Is Erroneous Because Lin and Parat Would Not Be Combined By A Person of Ordinary Skill

Claims 10-33 and 35-42 were rejected over various combinations of references, with all of the combinations involving both U.S. Pat. 6,057,207 to Lin et al. and U.S. Pat. 6,194,784 to Parat et al. (hereinafter "Lin" and "Parat"). It is respectfully submitted that the combination of Lin and Parat

is erroneous, and hence that all of the rejections must be withdrawn.

1. Lin and Parat involve completely different steps in the fabrication of semiconductor devices.

A person of ordinary skill would not combine Lin and Parat because the two references involve completely different problems, structures, and process steps in the fabrication of semiconductor devices.

In particular, the Examiner states at page 3, in paragraph 2, that "both Lin and Parat are directed to method of forming gate having stacked layer . . . ." This is not correct. Lin is directed to "a method for fabricating a planarized oxide layer [40] filling shallow trenches [30] in a substrate." Col. 2, line 1 et seq. Lin is not directed to a "method of forming gate having stacked layer," as the Examiner states. The word "gate" never even appears in Lin. Lin's raised portions 12A, 12B are not gates, but rather are the locations where active areas will be formed. The layers 24 and 20 ultimately are removed, as shown in Lin's Fig. 8.

By contrast, Parat involves the formation of a contact 220 to a diffusion region 212 between adjacent gate stacks 235. See Abstract and Col. 4, lines 8-25. Parat does not involve shallow trench isolation or chemical mechanical polishing, and never uses the words "shallow," "trench," "polish" or any variations thereof. Rather, Parat uses field oxide isolation regions instead of shallow trench isolation regions to isolate Parat's active regions, always etches, and never polishes. Col. 4, lines 51-55.

In sum, Lin and Parat address different problems, different structures, and different process steps. The formation of shallow trench isolation regions, as taught by Lin, is performed

in semiconductor processing well before the formation of the gates and contacts, as taught by Parat. Indeed, Parat states that, before Parat's process begins, the "silicon substrate 210 has been subjected to a local oxidation of silicon (LOCOS) isolation process which defines long narrow stripes of field oxide regions." This LOCOS process is an alternative to Lin's shallow trench isolation process.

Clearly, Parat adds nothing to Lin. The two references would never be combined by a person of ordinary skill addressing the problem faced by the inventors of the present application. Accordingly, the rejection of claims 10-33 and 35-42 should be withdrawn due to an improper combination of Lin and Parat.

2. Parat Provides No Motivation to Modify Lin's Process, and the Examiner's Proposed Modification Would Destroy Lin's Process.

The Examiner has focused on Parat's statement, at col. 6, line 50 et seq., that "[f]ollowing the encapsulation of the stack 235 in silicon nitride etch stop layer 238, an upper insulative or dielectric layer 221 is formed over the semiconductor device . . . ." This statement is not relevant to Lin's process. Hence, Parat provides no motivation to modify Lin's process.

In particular, Parat's process: (1) deposits and reflows a dielectric oxide layer 221 to achieve a planarized semiconductor device (col. 3:53-56); (2) then etches the oxide layer 221 selective to the nitride etch-stop layer 238 to form a contact opening 300 (col. 6:66 et seq.); and (3) then deposits metal to fill the contact opening 300 (col. 7:41 et seq.), thereby forming the contact 220. Parat's nitride etch stop layer 238 protects the gate stacks 235 during the etching of the contact opening 300. Col. 7, lines 3-6.

Lin is not concerned with forming contacts, as Parat is. Moreover, Lin fills his trenches 30 with oxide layer 40 before depositing the nitride etch barrier layer 44. Accordingly, there is no reason why Lin's process would be modified to include the formation of an additional oxide layer over Lin's nitride layer nitride etch barrier layer 44. The additional oxide layer proposed by the Examiner over Lin's etch barrier layer 44 would have no purpose in Lin's process. Adding Parat's oxide layer 221 It would be a waste of time and material, since Lin already filled his trenches with oxide layer 40, and ultimately would completely remove the additional oxide layer in Lin's first and second polishing steps. See Lin's Fig. 8.

In fact, Lin's process would be destroyed by the Examiner's proposed modification of Lin's process. Indeed, Lin's process depends on the presence of high areas 40A (Figs. 1-3), which extend higher than the adjacent planer portions of the oxide layer 40. Only the portions of nitride etch barrier layer 44 over the raised areas 40 are removed by Lin's first polishing step (Fig. 4), not the adjacent planar regions of nitride etch barrier layer 44). Accordingly, Lin's etch openings 50 are formed only over the wide raised portions 12A where the etch barrier layer 44 was removed.

If an additional reflowed dielectric layer like Parat's oxide layer 221 were deposited over Lin's nitride etch barrier layer 44, as the Examiner proposes, then Lin's high areas 40 would be covered, and could not be selectively polished in Lin's first etch step. Accordingly, Lin would not be able to form the openings 50, thereby destroying Lin's process.

Accordingly, the rejection of claims 10-33 and 35-42 should be withdrawn because Parat provides no reason to modify Lin's process.

B. The Rejection of Claims 11 and 30 Is Erroneous Because The Examiner's Combination Lacks a First Polish "to Expose Said First Nitride Layer"

The Examiner's proposed combination of Lin's process with Parat's oxide layer 221 does not include the feature of claims 11 and 30, namely, polishing the oxide "to expose said first nitride layer."

In particular, Lin's process requires that the first CMP step be stopped before the high portions 40A are obliterated and without removing the adjacent planar portions of nitride etch barrier layer 44, so that self aligned openings 50 may be formed over the wide raised portion 12A.

Hypothetically, if Lin's Fig. 4 were covered by Parat's oxide layer 221, as the Examiner proposes, Lin's first polishing step would not expose the planar regions of Lin's nitride etch barrier layer 44, since Lin's first CMP step must be stopped before the high portions 40A are obliterated. Accordingly, Parat's oxide layer 221 would remain over Lin's etch barrier layer 44, and the claimed feature of polishing the oxide "to expose said first nitride layer" would not be accomplished in any meaningful way.

Accordingly, claims 11 and 30 are not shown by the Examiner's combination.

C. Amendments to Claims 10 and 29

Claims 10 and 29 are amended to clarify the claims. It is the undersigned's view that the amendments do not reduce the scope of the claims.

In the Interview, the Examiner suggested that these amendments be made, notwithstanding that he found the arguments concerning the rejections to be persuasive.

CONCLUSION

It is submitted that claims 1-42 should be allowed. Reconsideration and allowance of the above-listed claims is respectfully requested.

If there are any questions, please telephone the undersigned at (408) 451-5906 to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 15, 2004.

3/15/04
Date

Signature: Rebecca A. Baumann